

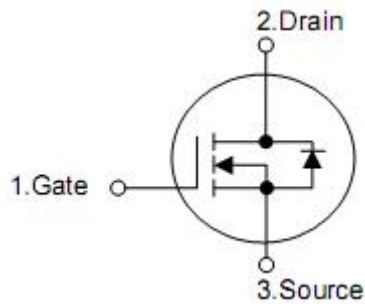
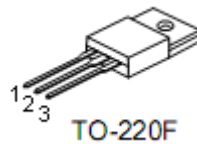
1. Features

- n Advanced Planar Process
- n $R_{DS(ON),(typ.)}=170m\Omega@V_{GS}=10V$
- n Low Gate Charge Minimize Switching Loss
- n Rugged Poly silicon Gate Structure

2. Features

- n BLDC Motor Driver
- n Electric Welder
- n High Efficiency SMPS

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNF7650A	TO-220F	KIA

5. Absolute maximum ratings

TC=25 °C unless otherwise specified

Parameter	Symbol	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}	500	V
Gate-to-Source Voltage	V_{GSS}	±30	
Continuous Drain Current	I_D	25	A
Continuous Drain Current @ $T_C=100\text{ °C}$		16	
Pulsed Drain Current at $V_{GS}=10V$ [2,4]	I_{DM}	100	
Single Pulse Avalanche Energy	E_{AS}	1800	mJ
Peak Diode Recovery dv/dt [3]	dv/dt	5.0	
Power Dissipation	P_D	105	W
Derating Factor above 25 °C		0.84	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	T_L T_{PAK}	300 260	°C
Operating and Storage Temperature Range	T_J & T_{STG}	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, junction-ambient	$R_{\theta JA}$	100	°C/W
Thermal resistance, Junction-case	$R_{\theta JC}$	1.19	

7. Electrical characteristics

(T_J=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	500	-	-	V
Drain-to-source Leakage Current	I _{DSS}	V _{DS} =500V, V _{GS} =0V	-	-	1	μA
		V _{DS} =400V, V _{GS} =0V T _C =125°C,	-	-	125	μA
Gate-body leakage current	I _{GSS}	V _{GS} =30V, V _{DS} =0V	-	-	+100	nA
		V _{GS} =-30V, V _{DS} =0V	-	-	-100	nA
On characteristics						
Static drain-source on-resistance	R _{DS(on)}	V _{GS} =10V, I _D =14A	-	170	210	Ω
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	-	4.0	V
Forward Transconductance	g _{fs}	V _{DS} =30V, I _D =14A	-	30	-	S
Dynamic characteristics						
Input capacitance	C _{iSS}	V _{DS} =25V, V _{GS} =0V, f=1MHz	-	4280	-	pF
Output capacitance	C _{oss}		-	1400	-	pF
Reverse transfer capacitance	C _{rSS}		-	185	-	pF
Total gate charge						
Turn-on delay time	t _{d(on)}	V _{DD} =250V, I _D =14A, V _{GS} =10V, R _G =10Ω	-	24	-	ns
Rise time	t _r		-	40	-	ns
Turn-off delay time	t _{d(off)}		-	100	-	ns
Fall time	t _f		-	35	-	ns
Total gate charge	Q _g	V _{DS} =250V, I _D =28A, V _{GS} =0 to 10V	-	76	-	nC
Gate-source charge	Q _{gs}		-	20	-	nC
Gate-drain charge	Q _{gd}		-	19	-	nC
Drain-source diode characteristics						
Drain-source diode forward voltage	V _{SD}	V _{GS} =0V, I _S =18A	-	-	1.5	V
Continuous drain-source current ^[2]	I _{SD}	Integral pn-diode In MOSFET	-	-	25	A
Pulsed drain-source current ^[2]	I _{SM}		-	-	100	A
Reverse recovery time	t _{rr}	V _{GS} =0V, I _F =28A	-	530	-	ns
Reverse recovery charge	Q _{rr}	DI _F /dt=100A/μs	-	4.5	-	μC

Note: 1. T_J=+25°C to +150°C

2. Silicon limited current only.

3. Package limited current

4. Repetitive rating; pulse width by maximum junction temperature

5. Pulse width ≤ 380μs; duty cycle ≤ 2%

8. Typical Characteristics

Figure 1. Maximum Transient Thermal Impedance

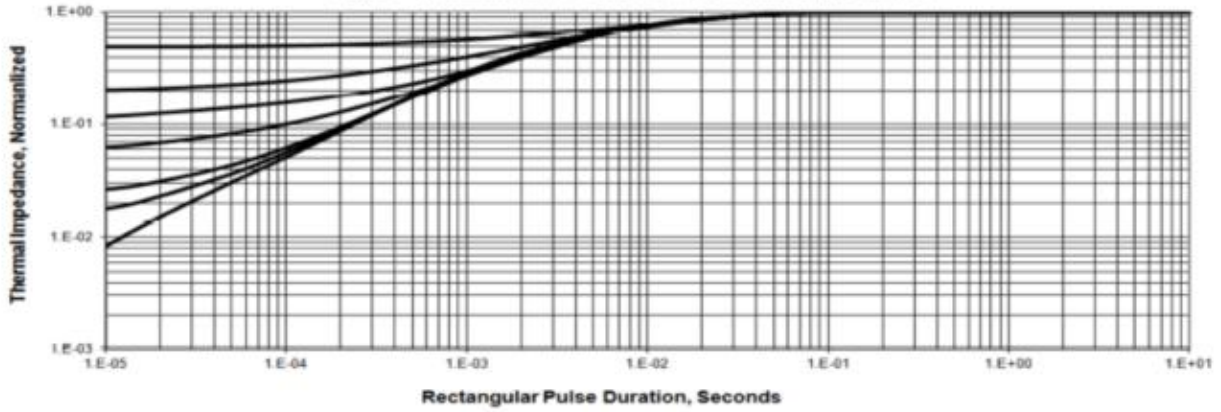


Figure 2 . Max. Power Dissipation vs Case Temperature

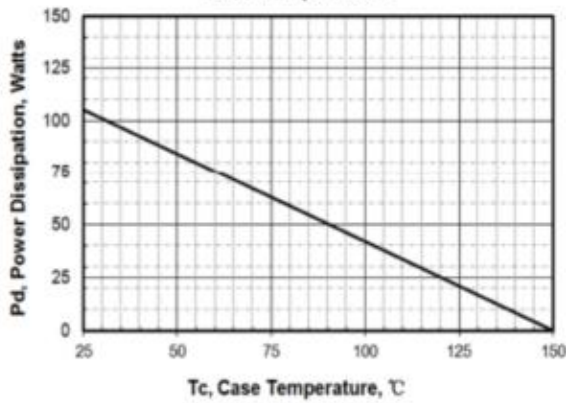


Figure 3 .Maximum Continuous Drain Current vs Tc

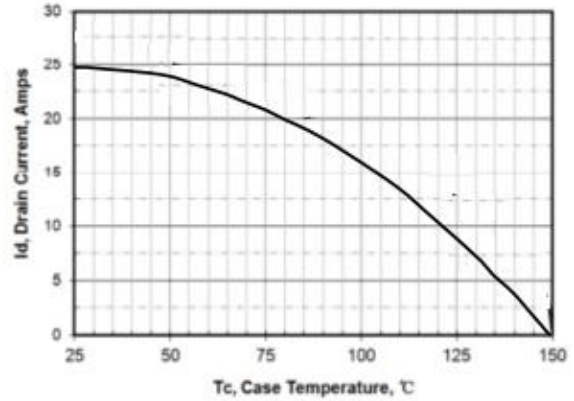


Figure 4. Output Characteristics

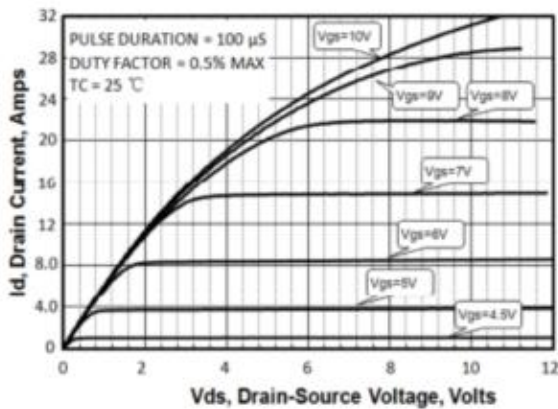


Figure 5. Rds(on) vs Gate Voltage

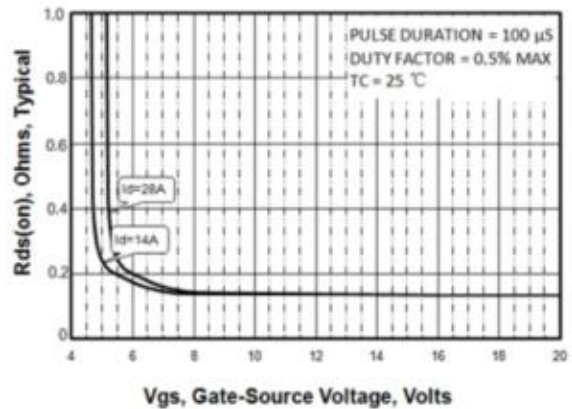


Figure 6. Peak Current Capability

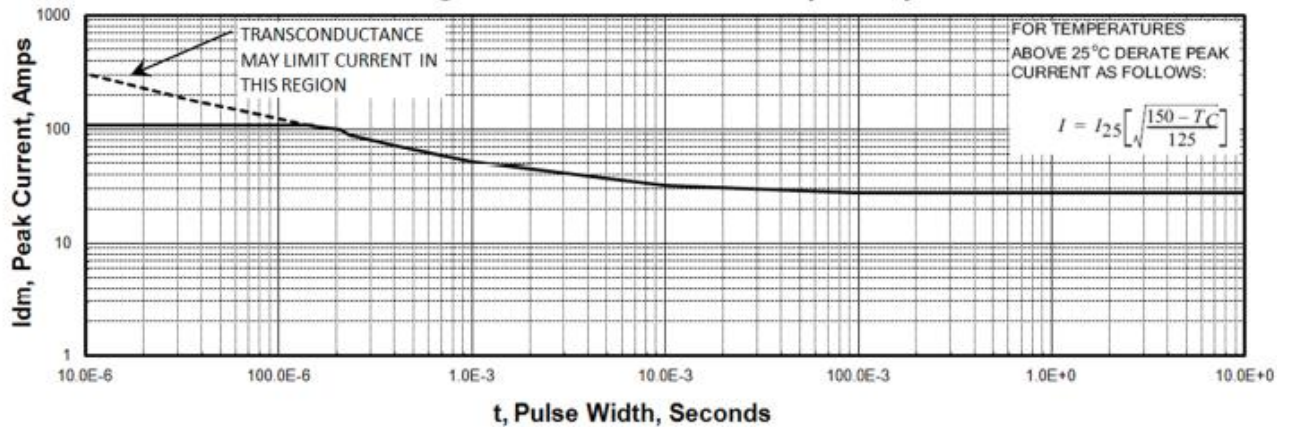


Figure 7. Transfer Characteristics

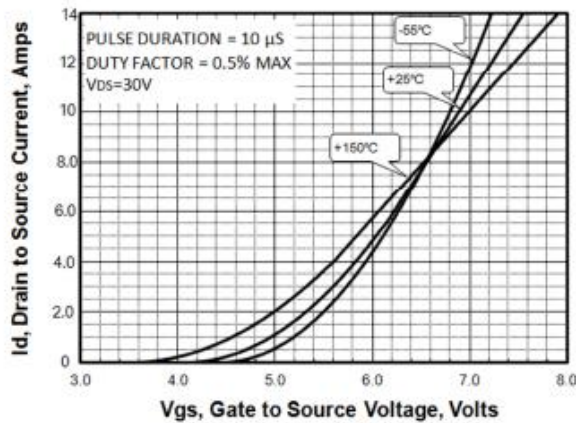


Figure 8. Unclamped Inductive Switching Capability

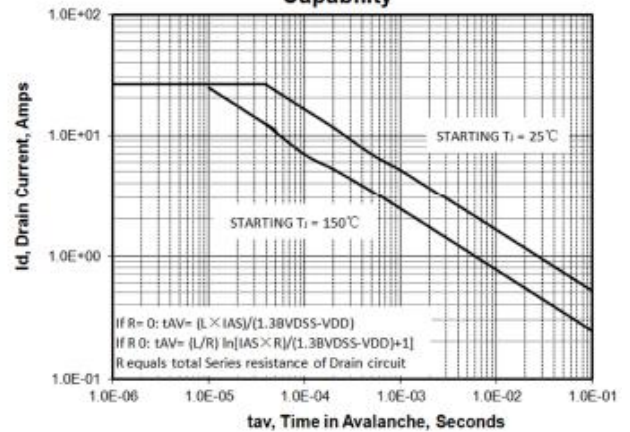


Figure 9. Drain to Source ON Resistance vs Drain Current

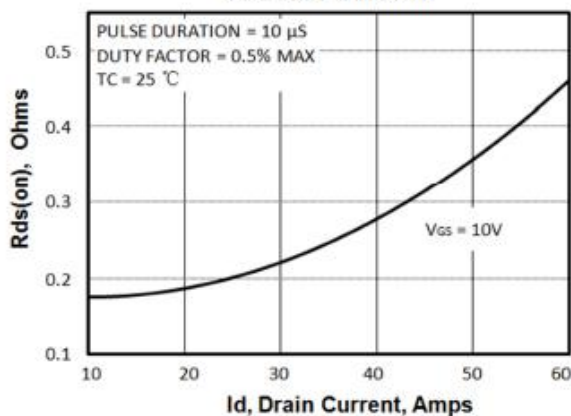


Figure 10. Rds(on) vs Junction Temperature

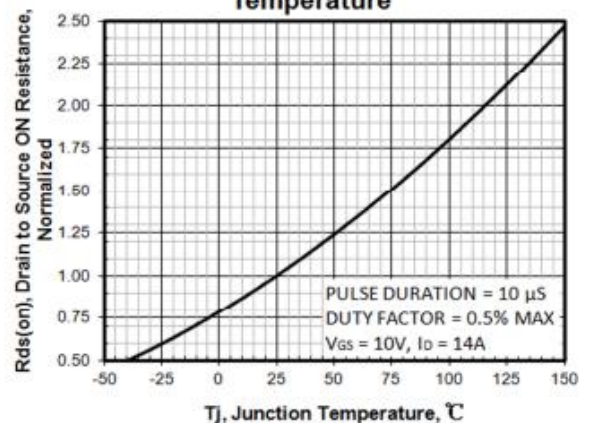


Figure 11. Breakdown Voltage vs Temperature

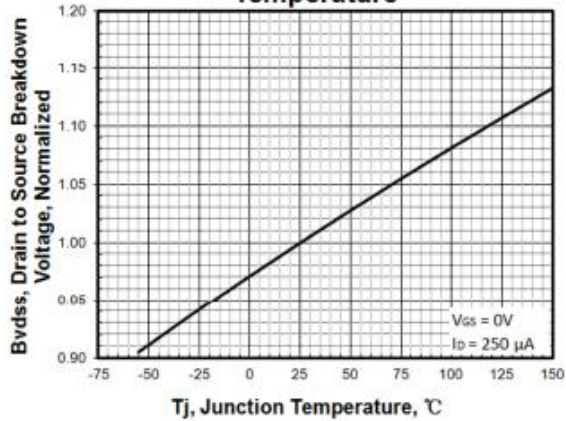


Figure 12. Threshold Voltage vs Temperature

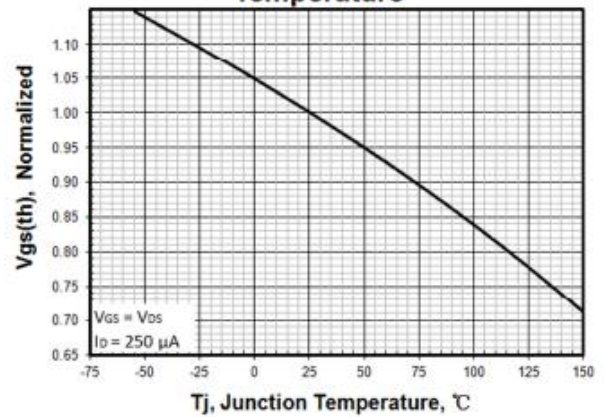


Figure 13. Maximum Safe Operating Area

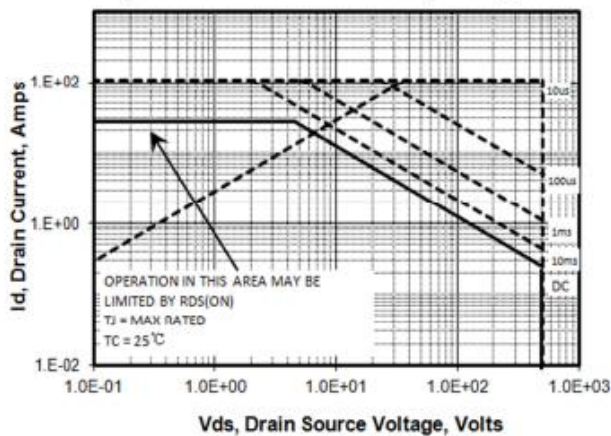


Figure 14. Capacitance vs Vds

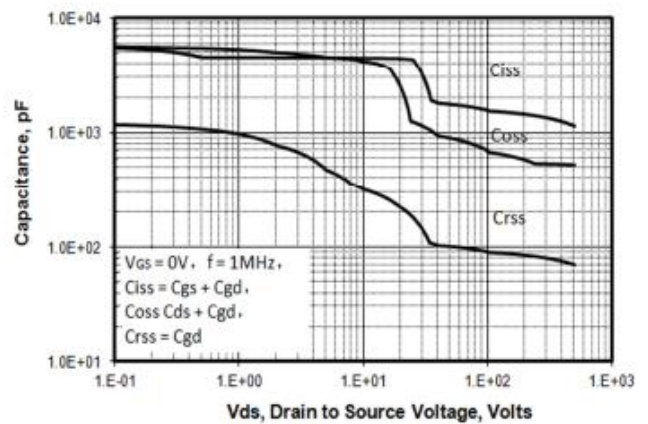


Figure 15. Typical Gate Charge

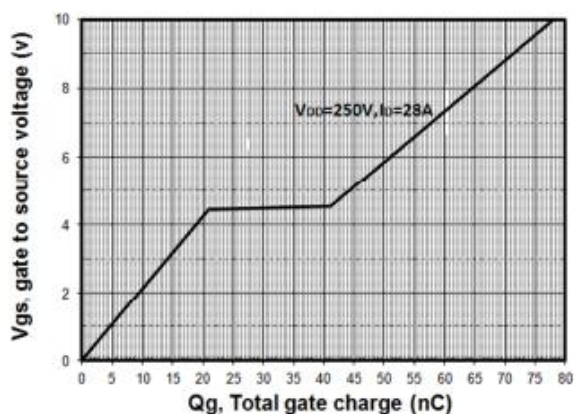
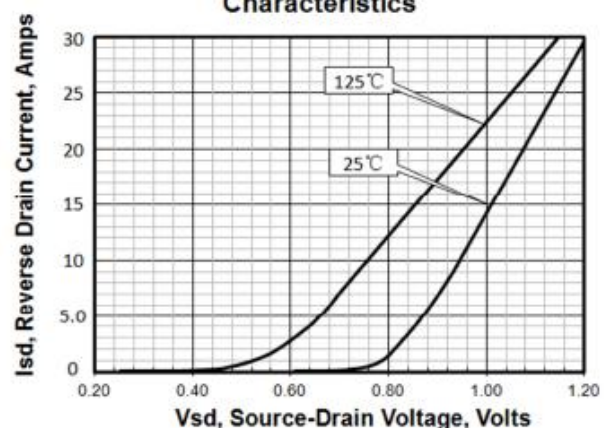


Figure 16. Body Diode Transfer Characteristics



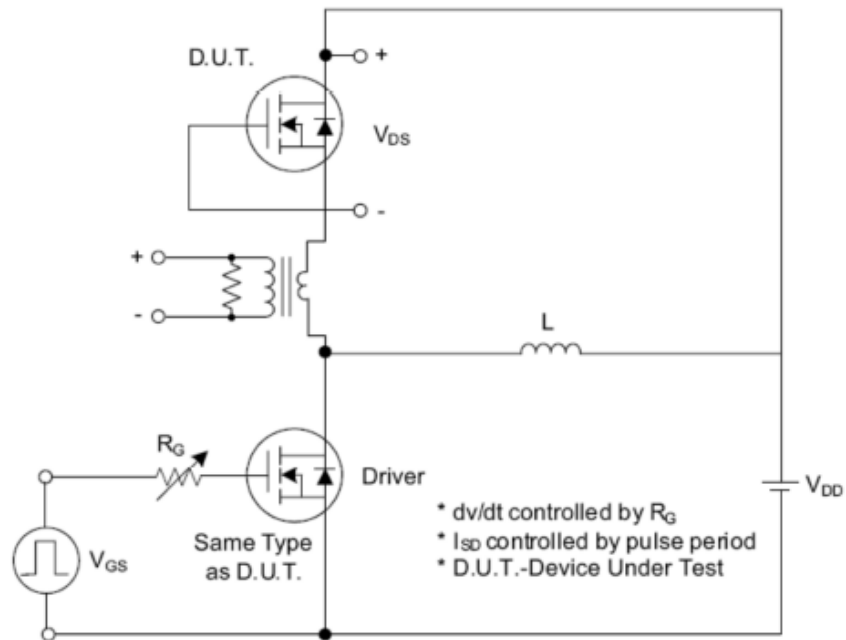


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

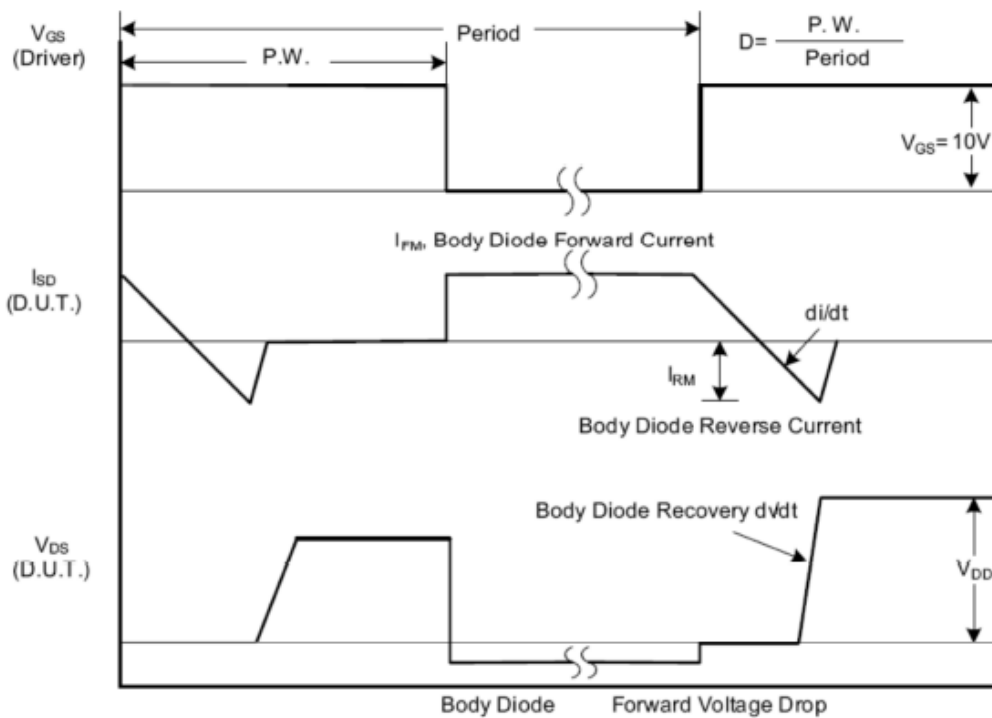


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

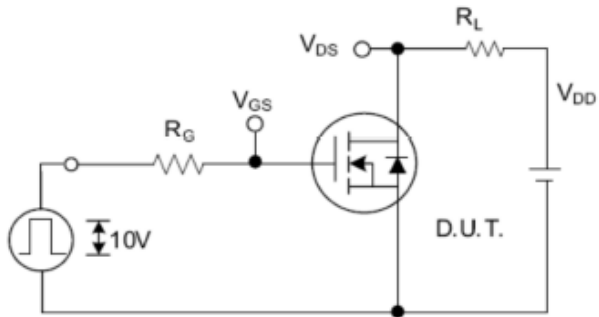


Fig. 2.1 Switching Test Circuit

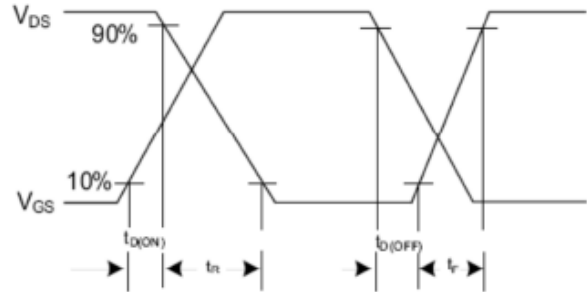


Fig. 2.2 Switching Waveforms

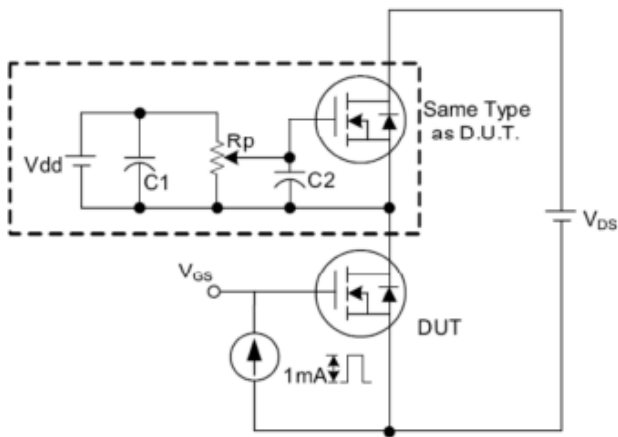


Fig. 3.1 Gate Charge Test Circuit

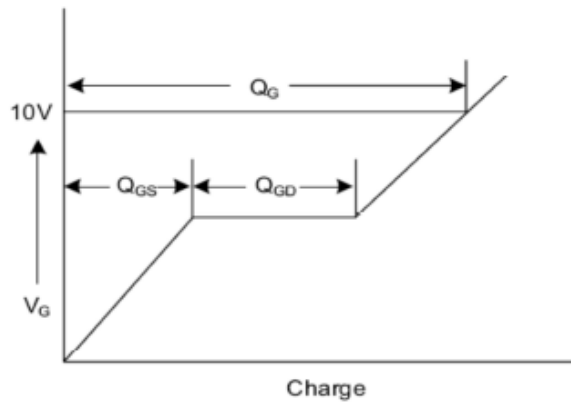


Fig. 3.2 Gate Charge Waveform

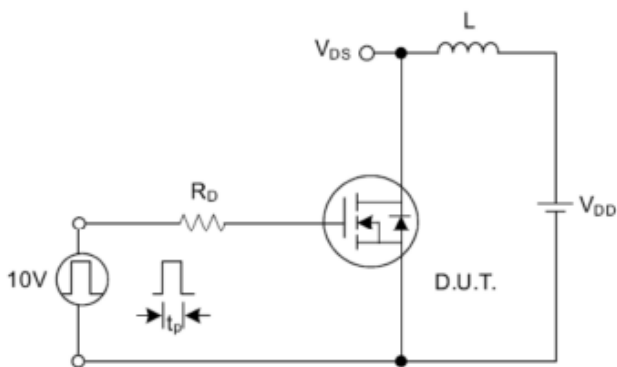


Fig. 4.1 Unclamped Inductive Switching Test Circuit

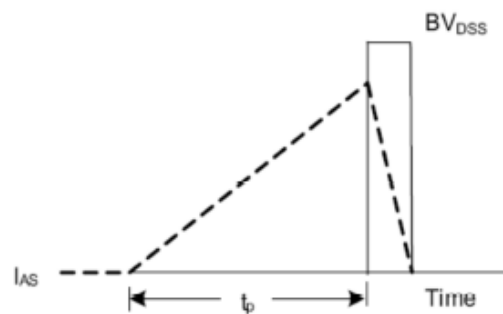


Fig. 4.2 Unclamped Inductive Switching Waveforms