

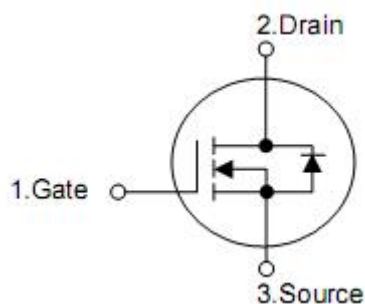
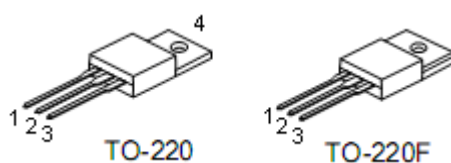
1. Description

These N-Channel enhancement mode power field effect transistors are produced using KIA's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies and electronic lamp ballasts based on half bridge.

2. Features

- n 4.5A,600V, $R_{DS(ON)} = 2.0\Omega @ V_{GS} = 10V$
- n Low c_{rss} (typ 8.0pF)
- n Low gate charge (typ $Q_g = 16nC$)
- n Fast switching
- n 100% avalanche tested
- n Improved dv/dt capability
- n RoHS compliant

3. Pin configuration



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

4. Absolute maximum ratings

(TC= 25 °C , unless otherwise specified)

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DSS}	600	V
Drain current	I_D	Tc=25 °C	4.5
		Tc=100 °C	2.7
Drain current pulsed (note 1)	I_{DM}	18	A
Gate-source voltage	V_{GSS}	±30	V
Single pulsed avalanche energy (note 2)	E_{AS}	116	mJ
Avalanche current (note 1)	I_{AR}	4.5	A
Repetitive avalanche energy (note 1)	E_{AR}	5.0	mJ
Peak diode recovery dv/dt (note 3)	dv/dt	4.5	V/ns
Power dissipation	P_D	Tc=25 °C	50
		derate above 25 °C	0.4
Operating and Storage temperature range	T_J, T_{STG}	-55 ~ +150	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	T_L	300	°C

5. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance, Junction-to-case	$R_{\theta JC}$	2.3	°C/W
Thermal resistance, Junction-to-ambient	$R_{\theta JA}$	83	°C/W

6. Electrical characteristics

(T_J=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Off characteristics						
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA, T _J =25°C	600			V
		V _{GS} =0V, I _D =250μA, T _J =150°C		630		V
Breakdown voltage temperature coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, referenced to 25 °C		0.6		V/°C
Zero gate voltage drain current	I _{DSS}	V _{DS} =600V, V _{GS} =0V			1	μA
		V _{DS} =480V, T _C =125 °C			10	μA
Gate-body leakage current	Forward	I _{GSSF}			100	nA
	Reverse	I _{GSSR}			-100	nA
On characteristics						
Gate threshold voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0		4.0	V
Static drain-source on-resistance	R _{DS(on)}	V _{GS} =10V, I _D =2.7A		2.0	2.5	Ω
Forward transconductance	g _{FS}	V _{DS} =40V, I _D =2.25A (note 4)			10	S
Dynamic characteristics						
Input capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		780		pF
Output capacitance	C _{oss}			70		pF
Reverse transfer capacitance	C _{rss}			8		pF
Switching characteristics						
Turn-on delay time	t _{d(on)}	V _{DD} =300V, I _D =4.5A, R _G =10Ω R _D =60Ω, V _{GS} =10V (note4,5)		12	30	ns
Turn-on rise time	t _r			40	90	ns
Turn-off delay time	t _{d(off)}			47	95	ns
Turn-off fall time	t _f			22	55	ns
Total gate charge	Q _g	V _{DS} =300V, I _D =4.5A, V _{GS} =10V, (note4,5)		16		nC
Gate-source charge	Q _{gs}			4.5		nC
Gate-drain charge	Q _{gd}			7		nC
Drain-source diode characteristics and maximum rating						
Maximum continuous drain-source diode forward current	I _S				4.5	A
Maximum pulsed drain-source diode forward current	I _{SM}				18	A
Drain-source diode forward voltage	V _{SD}	V _{GS} =0V, I _S =2.25A			1.5	V
Reverse recovery time	t _{rr}	V _{GS} =0V, I _S =4.5A		295		ns
Reverse recovery charge	Q _{rr}	di/dt=100A/μs (note4)		2.7		μC

- Note: 1. repetitive rating: pulse width limited by maximum junction temperature
 2. I_{AS}=4.5A, L=11.5mH, V_{DD}=50V, R_G=25Ω, starting T_J=25°C
 3. I_{SD}≤4.5A, di/dt≤100A/μs, V_{DD}≤BV_{DSS}, starting T_J=25 °C
 4. Pulse test: pulse width≤300μs, duty cycle≤2%
 5. Essentially independent of operating temperature Typical characteristics

7. Test circuits and waveforms

Figure 1. On-Region Characteristics

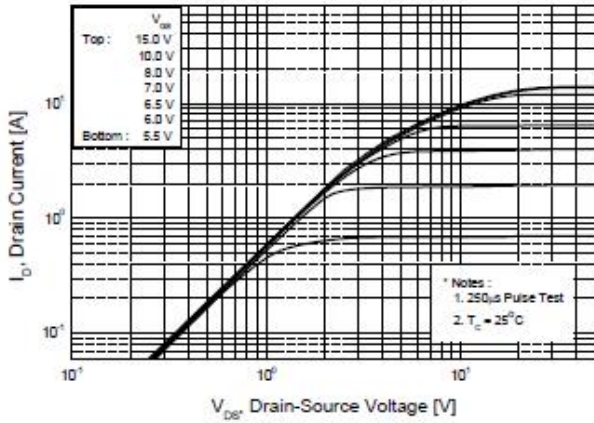


Figure 2. Transfer Characteristics

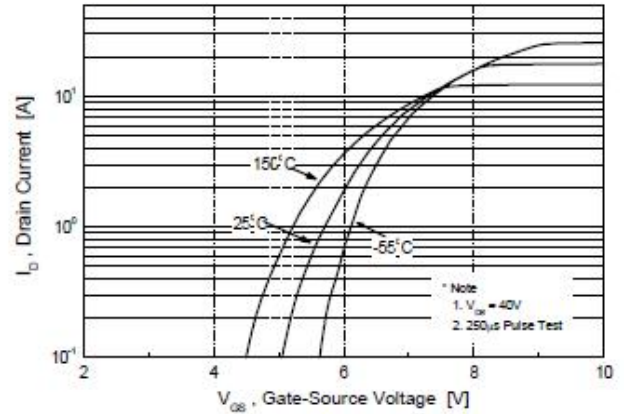


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

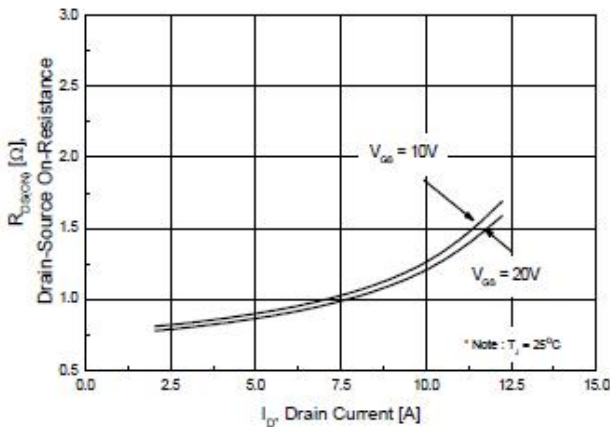


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

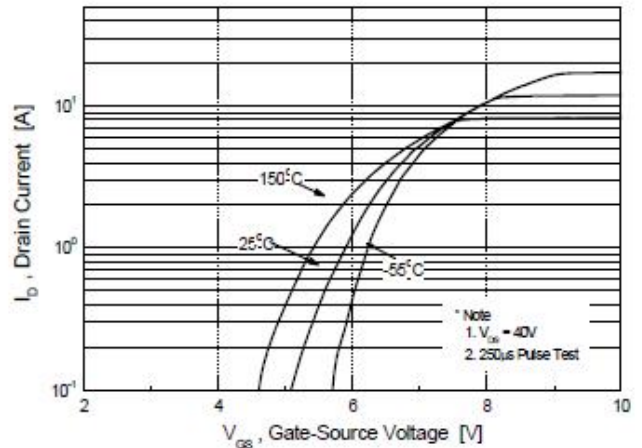


Figure 5. Capacitance Characteristics

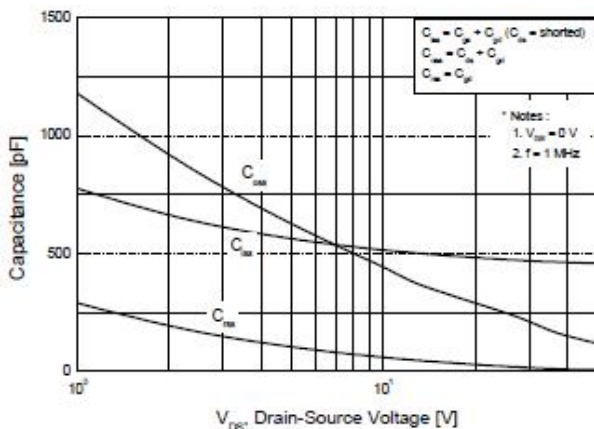


Figure 6. Gate Charge Characteristics

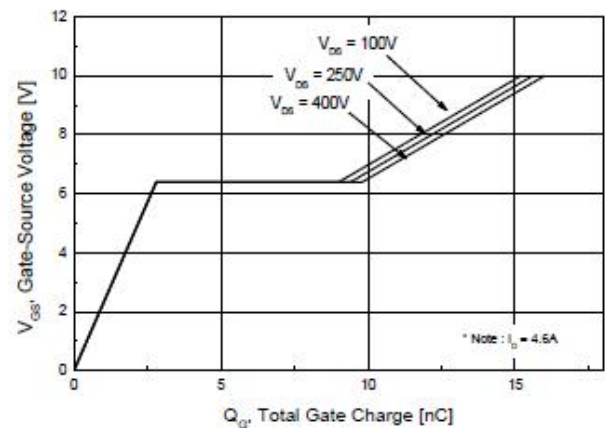


Figure 7. Breakdown Voltage Variation vs. Temperature

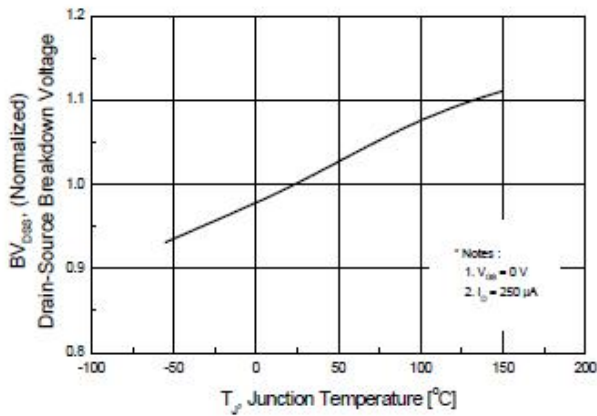


Figure 8. On-Resistance Variation vs. Temperature

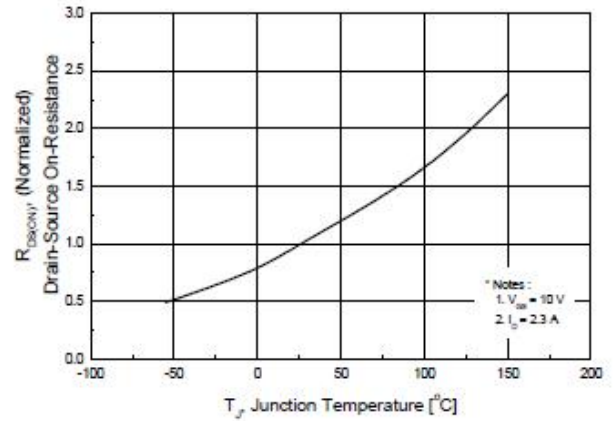


Figure 9. Maximum Safe Operating Area

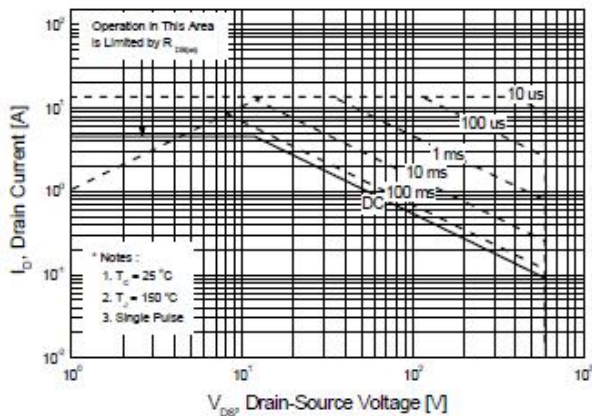


Figure 10. Maximum Drain Current vs. Case Temperature

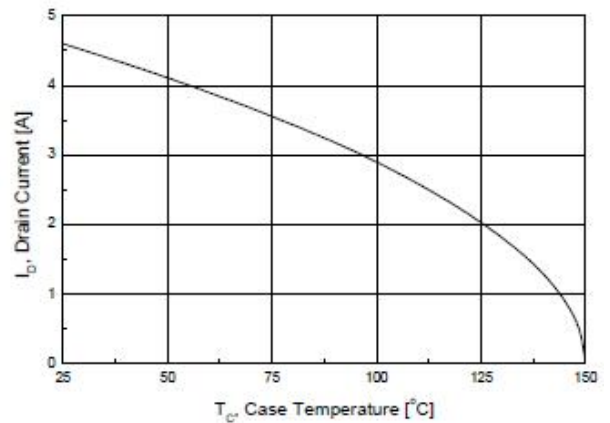
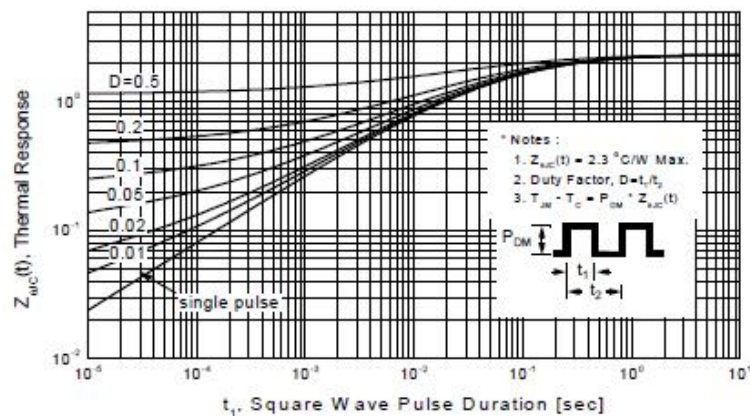
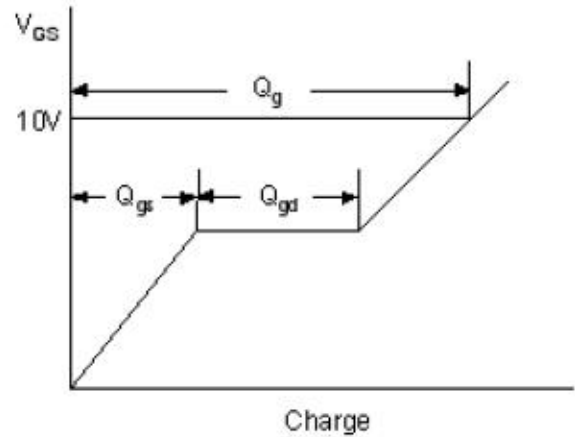
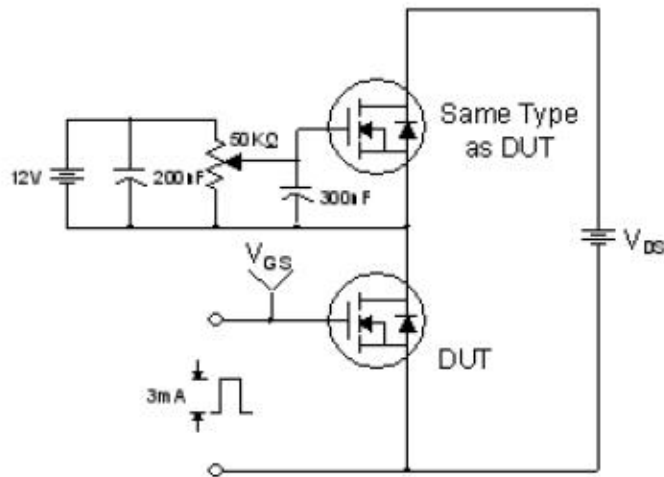


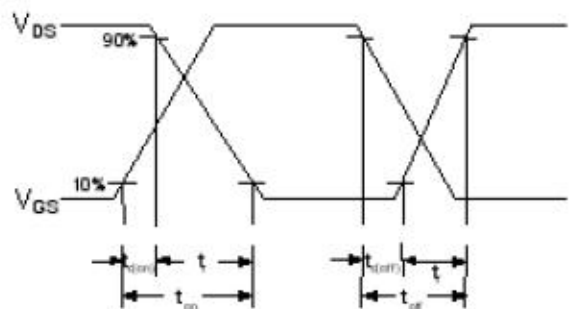
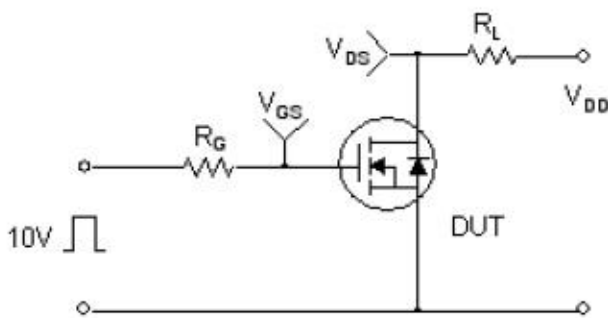
Figure 11. Transient Thermal Response Curve



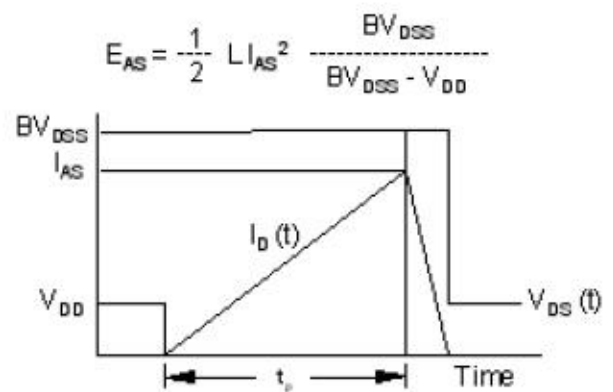
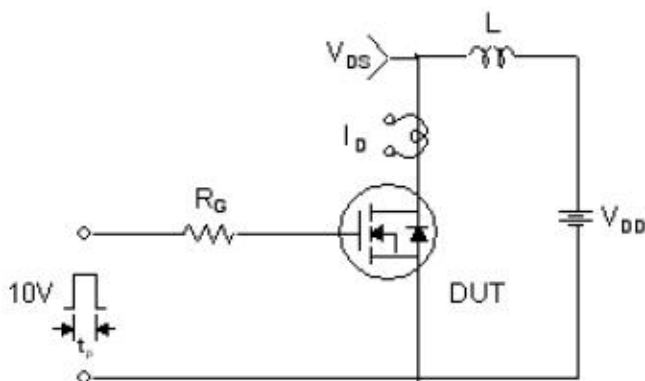
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

